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| EXAMINER |
|---|
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| 2826 | |

DATE MAILED: 04/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/863,030 | AMMAR, DAN F. | |
| | Examiner | Art Unit | |
| | Johannes P Mondt | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Amendment*

Amendment A filed 01/28/2003 and entered as Paper No. 11 forms the basis of this office action. In Amendment A Applicant substantially amended independent claims 1, 10, 16 and 26, and thereby all outstanding claims. Comments on Remarks by Applicant included below under "Response to Arguments" are therefore restricted to those aspects that are pertinent to the new claims.

### *Response to Arguments*

Remarks by Applicant have been full considered but are not persuasive. In particular:

(a) In connexion with the primary reference, Chan et al (5,451,818), Applicant states that "none of the cited references are primarily concerned with a transceiver"; however, Chan et al (5,451,818) does comprise the application of microelectronic packaging technology as disclosed to "all types of military and commercial applications [of MMIC (= monolithic microwave integrated circuit) technology that require low radio frequency (RF) losses at high operating frequencies" (cf. column 1, lines 11-20); it is understood in the art that said losses potentially play a role in both transmission and reception. Furthermore, the additional and new further limitation essentially requiring said previously called transfer tape to be a co-fired ceramic material is satisfied in Chan et al (cf. column 2, lines 54-66). The additional and new further limitation that the MMIC

chips be directly attached to the substrate board is implied in the alternatives for attachment indicated by Chan et al (cf. column 3, lines 33-40). That the capacitors and resistors must connect to the MMIC chip is inherent in MMIC transceivers; this is also independently clear from Moe et al (cf. abstract).

(b) The cited Wong reference is only cited for a specific teaching, i.e., efficiently connecting MMIC chips at low cost through a solder connection, and only the teaching by Wong in this regard needs to be combined with the invention by Chan et al. Motivation for doing so, and reasons for combinability and expectation of success for the implementation of said combination are indicated in the previous office action (cf. page 6 of Paper No. 9).

(c) The cited Moe et al reference is a patent on the fabrication of a MMIC hybrid device and transceiver fabricated therein, and therefore is related art. Furthermore, Moe et al is cited for a particular aspect of the invention, namely the thickness range of the base plate, while Applicant does not explain the critical nature of the claimed range in this regard in the specification.

(d) The cited Baudet reference is a patent on the soldering of a semiconductor device on a support. The examiner has applied said Baudet reference exclusively to the teaching of how to attach a MMIC device onto a substrate. The teaching in this regard is pertinent to the limitation lacking in the primary reference.

(e) The cited Osika reference teaches the trenches to extend down to the ground layer, although not through it (but that is not the claim language).

(f) The Douriet reference only has been cited for specific teaching, not for teaching the invention.

All other aspects of Remarks in said Amendment A refer to newly introduced limitations.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 10 and 15*** rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al (5,451,818).

*With regard to claim 10:* Chan et al teach (cf. Figure 1) a multi-layer substrate board used in transceiver modules comprising:

a plurality of low temperature transfer tape layers 15/20, said layers comprising one of at least: a layer with DC signals lines with signal tracks and connections 38 embedded by virtue of being formed by etching (cf. Figure 1 and column 3, line 58 – 68);

a ground layer 15 having ground connections (cf. column 2, lines 54 – 66); a device layer having capacitors and resistors therein connected to said MMIC chips (said capacitors and resistors are inherent in the MMIC chip that is preferably the selection for

the electronic devices 30a and 30b (cf. column 3, lines 24 – 40), and so is their connection to said MMIC chips);

a top layer having cutouts for receiving MMIC chips therein (column 2, lines 54-66); and

a solder perform layer located between said device layer and said top layer for securing any MMIC chips received within the top sheet (the latter is not shown but that is not needed for only one of the listed layers has to be taught by Chan et al). In conclusion, Chan et al teach claim 10.

*With regard to claim 15:* said base plate as taught by Chan et al is formed from a CTE matched material, namely CuW (cf. column 2, lines 21-31).

## *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 1, 3, 5 and 7*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,451,818) in view of Moe et al (5,239,685), and, in the alternative, over Chan et al in view of Moe et al (loc.cit) and Hudson (US 2003/0043887 A1).

*With regard to claim 1:*

Chan et al teach (cf. Figure 1) a thick film millimeter wave transceiver module (cf. abstract) comprising:

a base plate 12 (cf. column 2, line 21 – 53);

a multi-layer substrate board (15, laminated layer 20) (cf. column 2, line 54 – column 3, line 24) formed from a plurality of layers of low temperature co-fired ceramic material (cf. column 2, lines 54-66) and received on said base plate and MMIC chips directly attached to the substrate board (cf. column 3, lines 30-40) comprising

*at least one of* a layer with DC signals lines with signal tracks and connections 38 (cf. Figure 1 and column 3, line 58 – 68);

a ground layer 15 having ground connections (cf. column 2, lines 54 – 66);

a device layer having capacitors and resistors therein (said capacitors and resistors are inherent in the MMIC chip that is preferably the selection for the electronic devices 30a and 30b (cf. column 3, lines 24 – 40) while in this inherent function they have to connect to said MMIC chips);

a top layer having cutouts for receiving MMIC chips therein (column 2, lines 54-66); and a channelization plate (top of 20) received over the multi-layer substrate board and having channels formed to receive MMIC chips 30a and 30b and provide isolation between receive and transmit signals;

a solder preform layer is made of solder metal while this metal connects to the metallic resistors and capacitors (cf. column 3, lines 1-8); as shown in Figure 4 of the application said solder is in direct contact with said resistors and capacitors, and since the nature of the metal is not limited in the present claim language the further limitation of a solder perform layer does not distinguish over the prior art;

a channelization plate 31 (cf. both parts on opposite sides of the channel indicated by numeral 31 in Figure 1; cf. column 3, line 35) received over the multi-layer substrate board and having channels formed to receive (i.e., within which are positioned) MMIC chips (such as 30a) and provide isolation between transmit and receive signals, as between all RF lines 18 (cf. Figure 1 and column 2, lines 62-66).

*Chan et al do not necessarily* (a) limit said isolation material to air; nor is there (b) any specific teaching of the existence of both transmit and receive signal lines; nor any specific teaching that the layers of the substrate board are "thick films". However, ad (a) the examiner takes official notice that air is a well-proven and widely used insulating material between RF lines: the usefulness of air as such stems from its low thermal conductivity and dielectric constant; in the alternative, Hudson provides explicit teaching of the use of air as insulation between transmit and receiver lines (cf. paragraph [0065]); while ad (b) transmit and receive lines must be present in the MMIC devices indicated as the scope of the invention in Chan et al (cf. column 1, lines 11-20), while Moe et al (5,239,685) teach a MMIC transceiver (cf. title and abstract), which inherently has both transmit and receive lines. The need for electrical isolation between RF lines is furthermore independent on whether said lines are transmit or receive lines, and instead only depends on the tolerance acceptable for interference between RF lines; finally, ad (c): the distinction between "layer" and "film" does not have any patentable weight; while the adjective "thick" is a relative term, and as such, i.e., without quantification, does not further limit the device.

*With regard to claim 3:* the thick film mm wave transceiver according to claim 1 as taught by Chan et al further comprises a radio frequency (namely: made of Kovar R) cover 28 (cf. abstract and column 3, lines 9-24).

*With regard to claim 7:* the base plate as taught by Chan et al is made of CuW (cf. column 2, lines 21-31), i.e., it is formed from a CTE matched material.

1. ***Claims 4-6 and 8-9*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Moe et al, (or, in the alternative, in view of Hudson as well, see rejection under 103(a) of claim 1) as applied to claim 1, and further in view of Shiau et al (5,319,329). Although Chan et al do not necessarily teach the further range limitations for the thicknesses of the layers of the multi-layer substrate board, it is noted that layer thicknesses of about 4 mils for dielectric substrate layers are well known in the field of Applicant's invention, as shown by Sjiau et al in a patent for a MMIC filter, who teach a dielectric gallium arsenide layer of about 4 mils thick (cf. column 2, lines 35-46). Furthermore, Applicant does not show in his disclosure why the further limitations define ranges critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

*With regard to claims 8-9:* Although Chan et al do not necessarily teach the further range limitations for the thickness of the base plate, it is noted that base plate thicknesses of about 0.64 mm (i.e., 0.16 inches) are well known in the field of MMIC devices, as shown by Moe et al (cf. column 5, line 3). Furthermore, Applicant does not disclose why the ranges defined in claims 8-9 are critical to his invention. Applicant is

reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

2. ***Claims 12-14*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,451,818) in view of Shiau et al (5,319,329). Although Chan et al do not necessarily teach the further range limitations for the thicknesses of the layers of the multi-layer substrate board, it is noted that layer thicknesses of about 4 mils for dielectric substrate layers are well known in the field of Applicant's invention, as shown by Sjiau et al in a patent for a MMIC filter, who teach a dielectric gallium arsenide layer of about 4 mils thick (cf. column 2, lines 35-46). Furthermore, Applicant does not show in his disclosure why the further limitations define ranges critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

3. ***Claim 16, 20, 23 and 26*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,451,818) in view of Wong et al (4,506,122).

*With regard to claim 16:* Chan et al teach (cf. Figure 1) a thick film millimeter wave transceiver module comprising:

a base plate 12 (cf. column 2, lines 21-31);

a multi-layer substrate board 15/20 (cf. column 2, line 54 – column 3, line 24 and please see comments in the rejection under 103(a) of claim 1 on the absence of patentable weight of the further limitation "thick film", herein incorporated by reference) received on said base plate and having a plurality of layers of co-fired ceramic material (cf. column 2, lines 54-66) and received on said base plate and MMIC chips directly attached to substrate board (cf. column 3, lines 30-40; said direct attachment is implied as one of the options delineated here), said layers comprising one of at least:

a DC signals layer having DC signals lines with signal tracks and connections 38 (cf. Figure 1 and column 3, line 58 – 68);

a ground layer 15 having ground connections (cf. column 2, lines 54 – 66);

a device layer having capacitors and resistors therein (said capacitors and resistors are inherently connected to the MMIC chip that is preferably the selection for the electronic devices 30a and 30b (cf. column 3, lines 24 – 40)) embedded therein (cf. column 3, lines 58-68);

a top layer having cutouts for receiving MMIC chips therein (column 2, lines 54-66);

a solder preform layer is made of solder metal while this metal connects to the metallic resistors and capacitors (cf. column 3, lines 1-8); as shown in Figure 4 of the application said solder is in direct contact with said resistors and capacitors, and since the nature of the metal is not limited in the present claim language the further limitation of a solder perform layer does not distinguish over the prior art; for all substantial device

purposes the term "solder perform layer" will thus henceforth be equated to said resistors and capacitors;

a channelization plate 31 (cf. both parts on opposite sides of the channel indicated by numeral 31 in Figure 1; cf. column 3, line 35) received over the multi-layer substrate board and having channels formed to receive (i.e., within which are positioned) MMIC chips (such as 30a) and provide isolation between transmit and receive signals, as between all RF lines 18 (cf. Figure 1 and column 2, lines 62-66).

at least one MMIC chip received on the solder perform layer and operatively connected to said layers, including said embedded DC signal tracks and connections and capacitors and resistors embedded in the device layer; and

and a channelization plate (top of 20) received over the multi-layer substrate board and having channels formed to receive MMIC chips 30a and 30b and provide isolation between receive and transmit signals;

*Chan et al do not necessarily teach* the at least one chip to be secured by a solder connection; however, solder connections for efficiently connecting MMIC chips at low cost are common in the art, as witnessed for instance by Wong et al (cf. column 2, lines 37-47), while the use of solder connections of the MMIC chips in Chan et al combines well with the extensive use of solder for connections in Chan et al (cf. column 2, line 32, column 3, line 13).

*Motivation* to include the teaching in this regard by Wong et al would thus be the use of a low cost method for connection already used in the manufacturing of the

device, thus ensuring the *combinability*. *Success* in implementing the combination can therefore be reasonably expected.

*With regard to claim 20:* as taught by Chan et al, the lid 28 received over the channelization plate is made of Kovar R (cf. column 3, lines 9-24).

*With regard to claim 23:* the base plate as taught by Chan et al is made of a CTE material, namely CuW (cf. column 2, lines 21-31).

*With regard to claim 26:* The device of claim 16 would necessarily have to be formed in order to function. Claim 26 fails to further limit the device of claim 16 other than simply form each of their components.

4. ***Claim 18*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 16 above, and further in view of Baudet (5,844,321). As detailed above, claim 16 is unpatentable over Chan et al in view of Wong et al. Neither Chan et al nor Wong et al necessarily teach the further limitation of claim 18. However, the use of solder perform has long been applied to the art of soldering chips to substrates, as evidenced by Baudet, who teaches the use of solder perform layers to solder chips to substrates (cf. abstract, final sentence).

5. ***Claims 21-22*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 16 above, and further in view of Shiau et al (5,319,329). Although Chan et al nor Wong et al necessarily teach the further range limitations for the thicknesses of the layers of the multi-layer substrate board, it is noted

that layer thicknesses of about 4 mils for dielectric substrate layers are well known in the field of Applicant's invention, as shown by Sjiau et al in a patent for a MMIC filter, who teach a dielectric gallium arsenide layer of about 4 mils thick (cf. column 2, lines 35-46). Furthermore, Applicant does not show in his disclosure why the further limitations define ranges critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

6. ***Claims 24-25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 23 above, and further in view of Moe et al (5,239,685). Although Chan et al nor Wong et al necessarily teach the further range limitations for the thickness of the base plate, it is noted that base plate thicknesses of about 0.64 mm (i.e., 0.16 inches) are well known in the field of MMIC devices, as shown by Moe et al (cf. column 5, line 3). Furthermore, Applicant does not disclose why the ranges defined in claims 8-9 are critical to his invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. ***Claim 2*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,541,818) and Moe et al (and, in the alternative, over Chan et al, Moe et al and

Hudson) as applied to claim 1, and further in view of Osika (5,254,941). As detailed above, claim 1 is unpatentable over Chan et al in view of Moe et al (or, in the alternative, over Chan et al in view of both Moe et al and Hudson). Chan et al do not necessarily teach the further limitations of claim 2. However, the use of isolation vias has long been known in the art of providing electrical isolation between active devices, such as are taught to be included in Chan et al (devices 30a and 30b), as is demonstrated by the patent to Osika, who discussed the need to provide electrical isolation of active devices through isolation vias and check said isolation (cf. abstract). Please note that said vias extend to the ground plane (cf. front figure in Osika).

*Motivation* to include the teaching by Osika is the need for active devices to be able to operate independently. The teaching in this regard by Osika can be easily *combined* by providing isolation trenches in the standard manner as already admitted in Applicant's disclosure, and as is also clear from Osika (cf. column 1, line 21-50). *Success* in the implementation can therefore reasonably be expected.

8. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,541,818) in view of Osika (5,254,941). As detailed above, Chan et al anticipate claim 10. Chan et al do not necessarily teach the further limitations of claim 11. However, the use of isolation vias has long been known in the art of providing electrical isolation between active devices, such as are taught to be included in Chan et al (devices 30a and 30b), as is demonstrated by the patent to Osika, who discussed the

need to provide electrical isolation of active devices through isolation vias and check said isolation (cf. abstract).

*Motivation* to include the teaching by Osika is the need for active devices to be able to operate independently. The teaching in this regard by Osika can be easily *combine*d by providing isolation trenches in the standard manner as already admitted in Applicant's disclosure, and as is also clear from Osika (cf. column 1, line 21-50). *Success* in the implementation can therefore reasonably be expected.

9. ***Claim 17*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 16 above, and further in view of Osika (5,254,941). As detailed above, claim 16 is unpatentable over Chan et al in view of Wong et al. Neither Chan et al nor Wong et al necessarily teach the further limitation of claim 17. However, the use of isolation vias has long been known in the art of providing electrical isolation between active devices, such as are taught to be included in Chan et al (devices 30a and 30b), as is demonstrated by the patent to Osika, who discussed the need to provide electrical isolation of active devices through isolation vias and check said isolation (cf. abstract). Please note that said visa extend to the ground plane.

*Motivation* to include the teaching by Osika is the need for active devices to be able to operate independently. The teaching in this regard by Osika can be easily *combined* by providing isolation trenches in the standard manner as already admitted in Applicant's disclosure, and as is also clear from Osika (cf. column 1, line 21-50). *Success* in the implementation can therefore reasonably be expected.

10. ***Claim 19*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 16 above, and further in view of Douriet et al (6,426,686 B1). As detailed above, claim 16 is unpatentable over Chan et al in view of Wong et al. Neither Chan et al nor Wong et al necessarily teach the further limitation defined by claim 19. However, as is evident from for instance Douriet et al (Figures 10 and 11 and column 6, lines 27-57), the use of silver epoxy for is standard in the art of providing efficient die attachment in integrated circuits.

## *Conclusion*

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
March 27, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800